

FIGURE 1 (Prior Art)

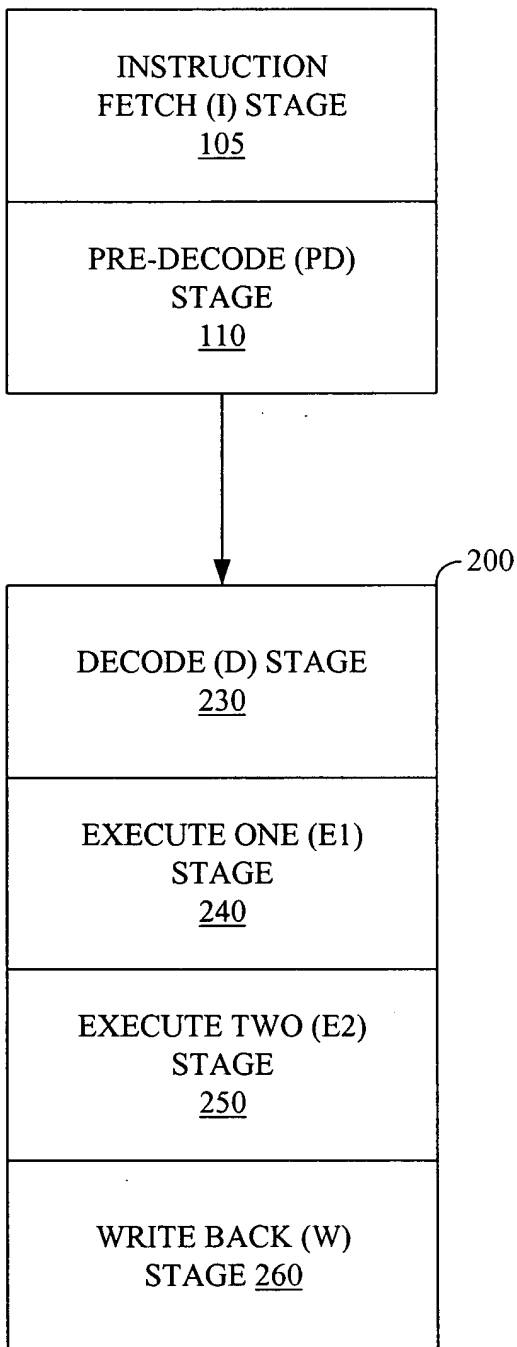


FIGURE 2 (Prior Art)

FIG. 3(a) is a block diagram of a processor 100 showing a pipeline 120 with four stages: D STAGE 130, E1 STAGE 140, E2 STAGE 150, and W STAGE 160. The D STAGE 130 performs an ADD D1, D0, #1 operation. The E1 STAGE 140 performs an LD D0, [A0] operation. The E2 STAGE 150 performs an LD D0, [A0] operation. The W STAGE 160 performs a write-back operation. The pipeline 120 is connected to a memory 200.

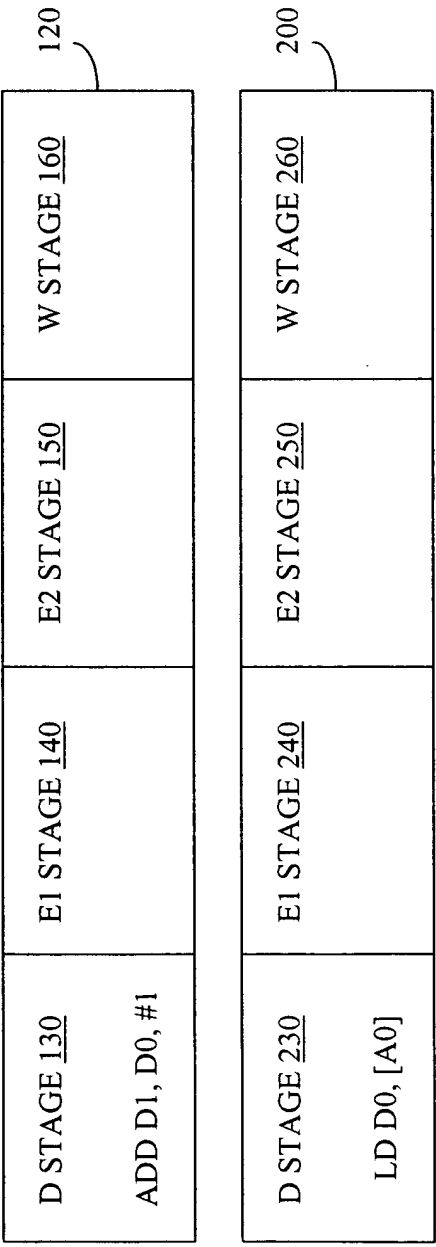


Figure 3(a)

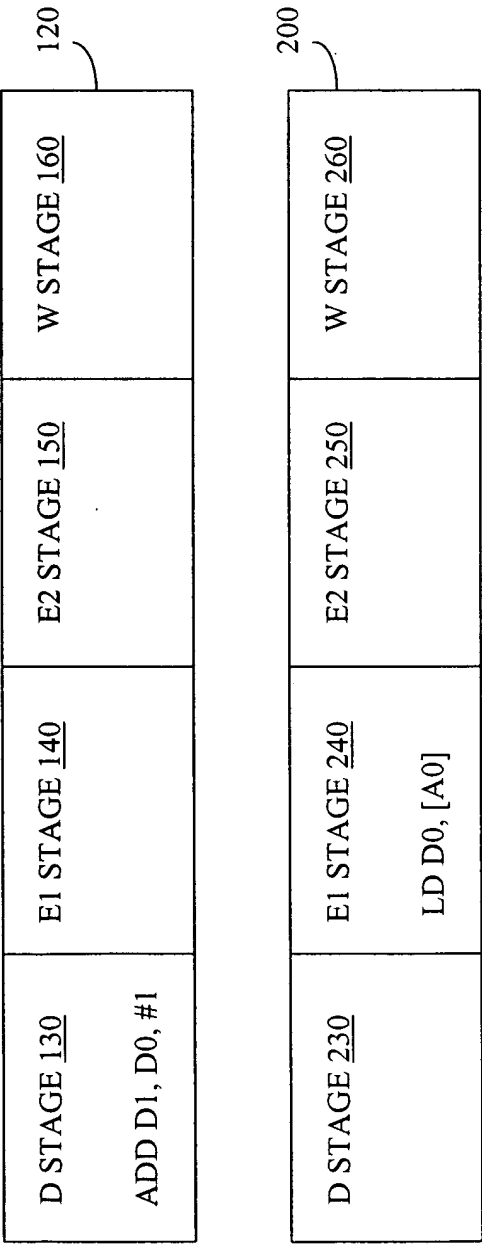


Figure 3(b)

FIG. 3(c) is a block diagram of a processor 100 in accordance with one embodiment of the present invention. The processor 100 includes a D stage 130, an E1 stage 140, an E2 stage 150, and a W stage 160. The D stage 130 is configured to add D1, D0, #1. The E1 stage 140 is configured to add D1, D0, #1. The E2 stage 150 is configured to add D1, D0, #1. The W stage 160 is configured to add D1, D0, #1.

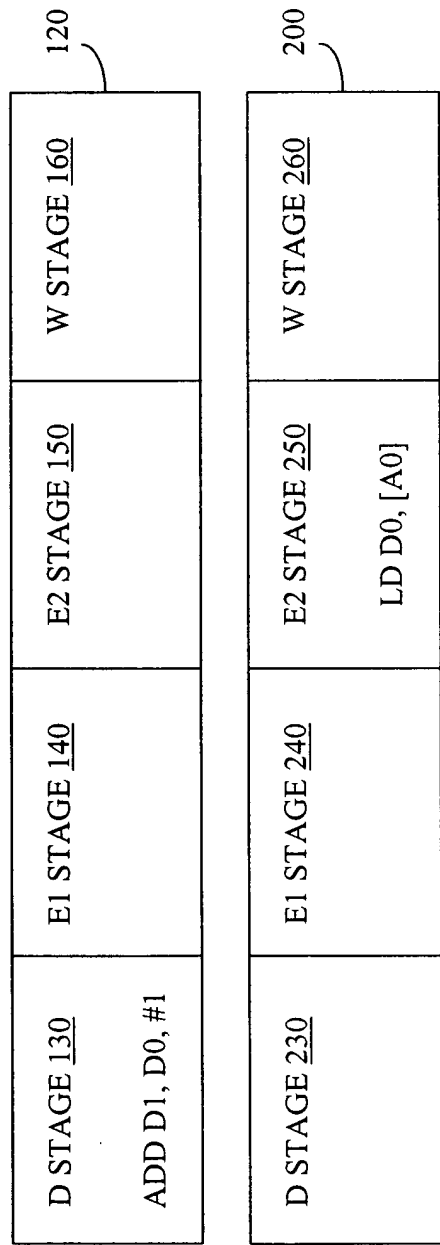


Figure 3(c)

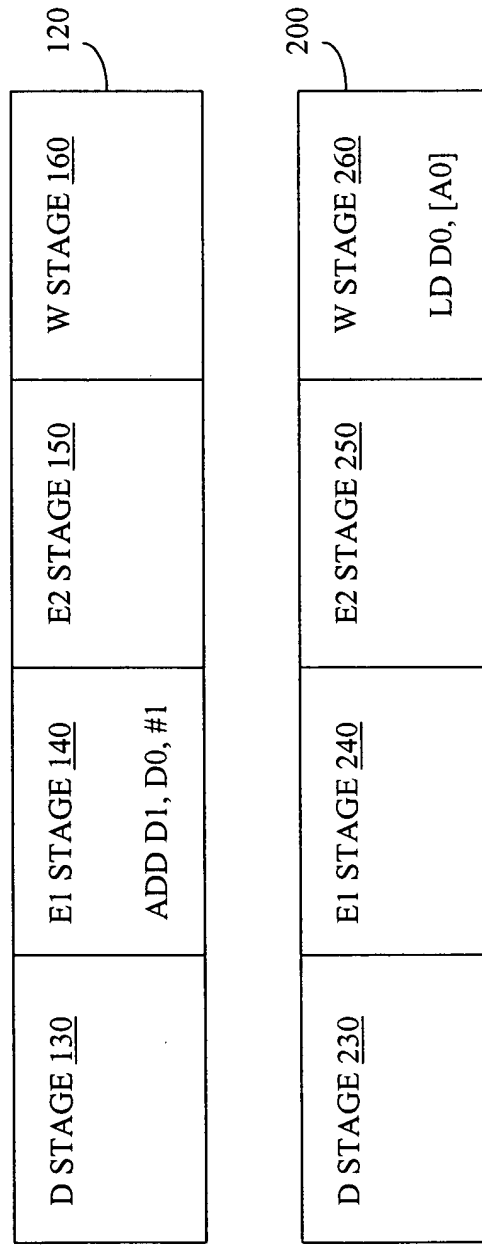


Figure 3(d)

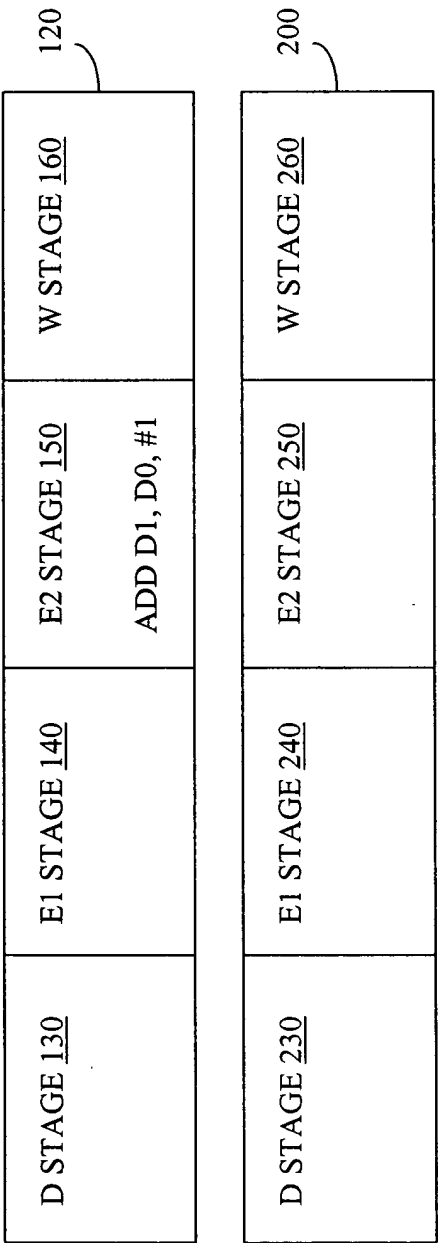


Figure 3(e)

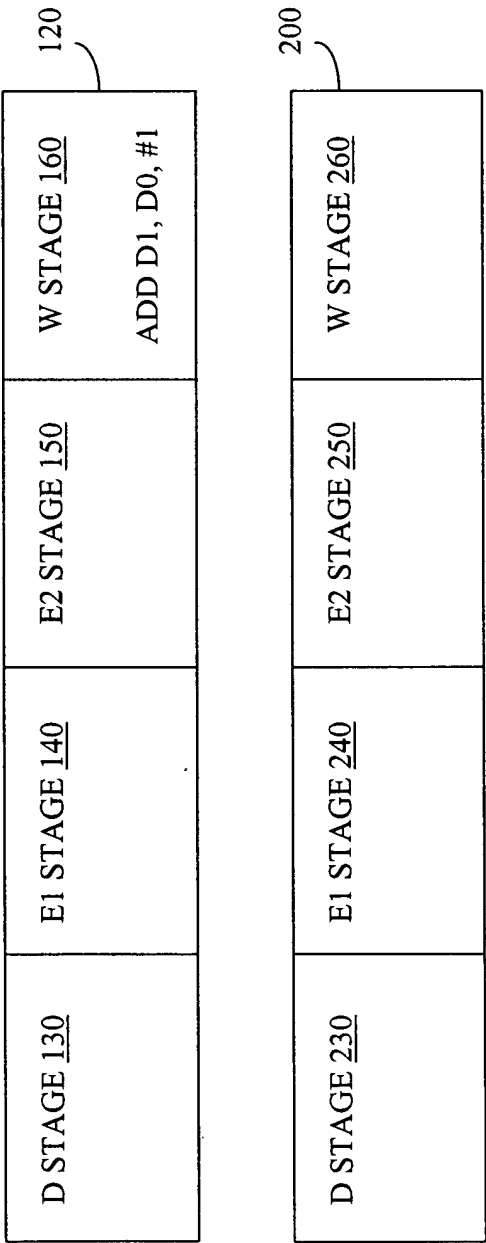
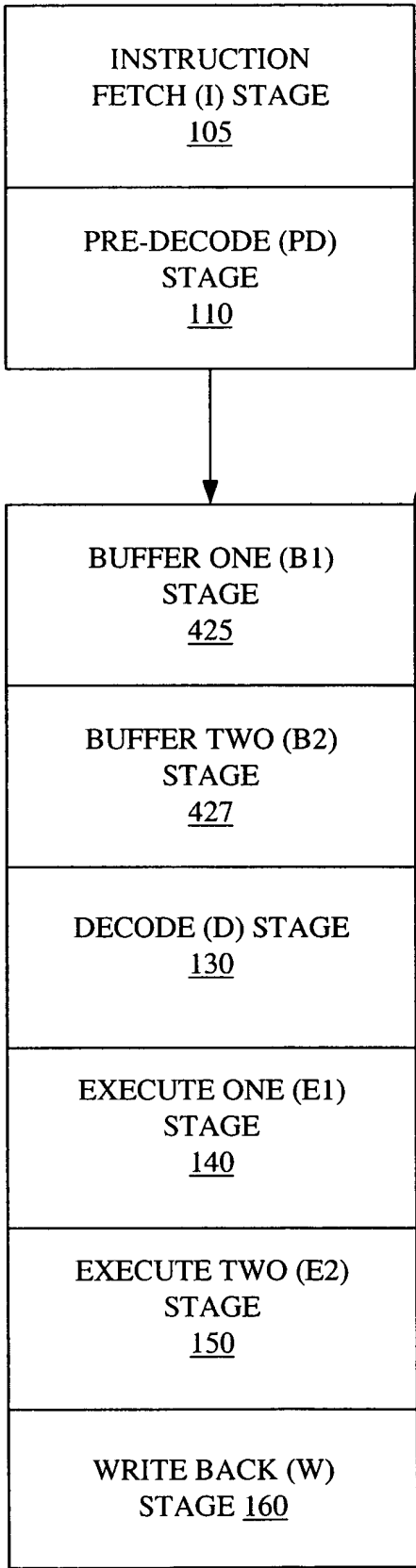


Figure 3(f)



400

FIGURE 4 (Prior Art)

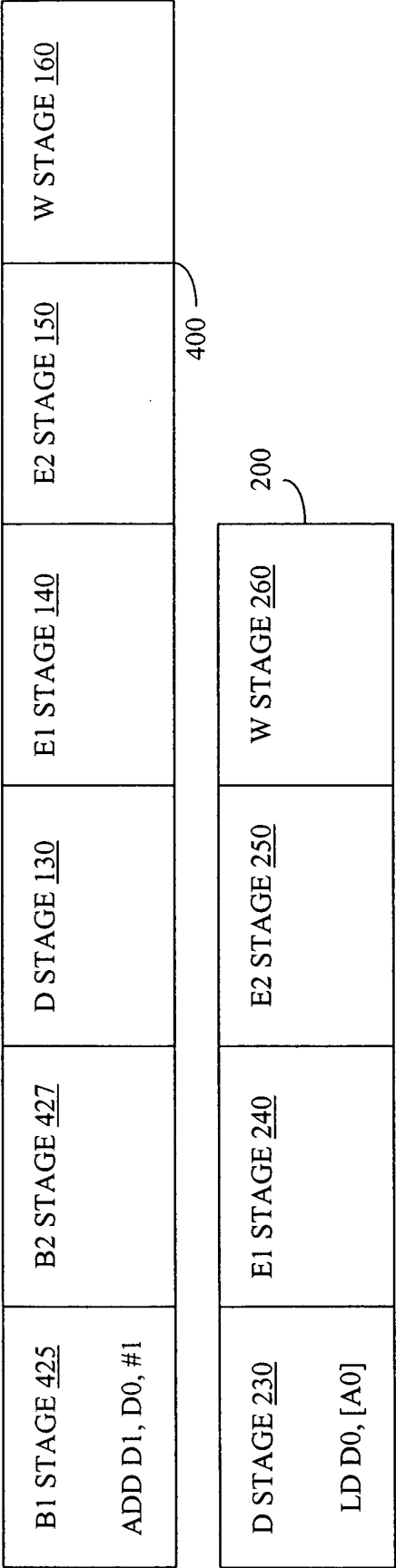


Figure 5(a)

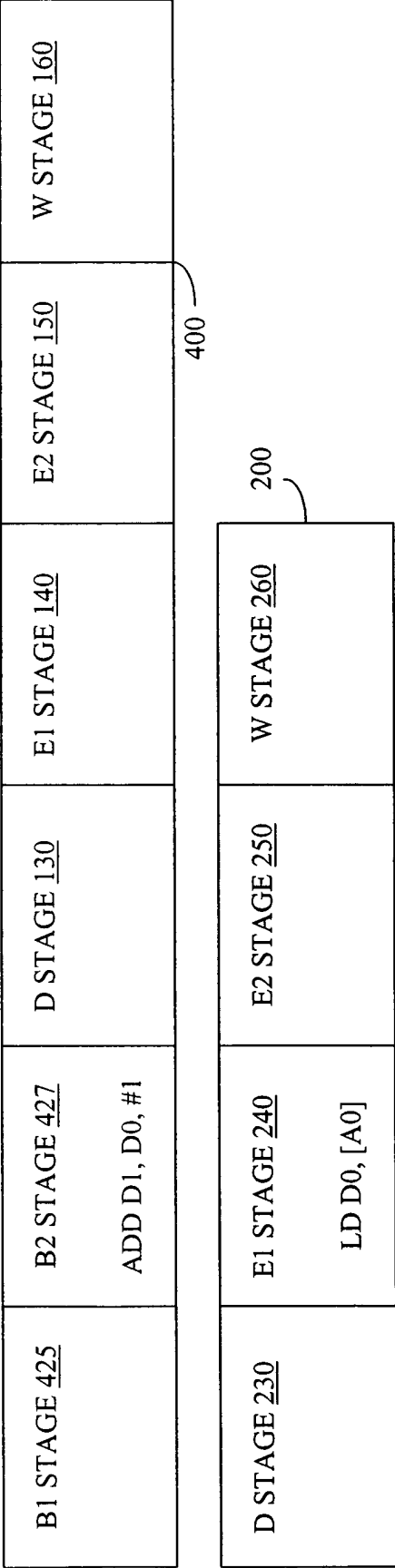


Figure 5(b)

B1 STAGE <u>425</u>	B2 STAGE <u>427</u>	D STAGE <u>130</u> ADD D1, D0, #1	E1 STAGE <u>140</u>	E2 STAGE <u>150</u>	W STAGE <u>160</u>
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400

D STAGE <u>230</u>	E1 STAGE <u>240</u>	E2 STAGE <u>250</u> LD D0, [A0]	W STAGE <u>260</u>
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200

B1 STAGE <u>425</u>	B2 STAGE <u>427</u>	D STAGE <u>130</u>	E1 STAGE <u>140</u> ADD D1, D0, #1	E2 STAGE <u>150</u>	W STAGE <u>160</u>
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400

D STAGE <u>230</u>	E1 STAGE <u>240</u>	E2 STAGE <u>250</u>	W STAGE <u>260</u> LD D0, [A0]
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200

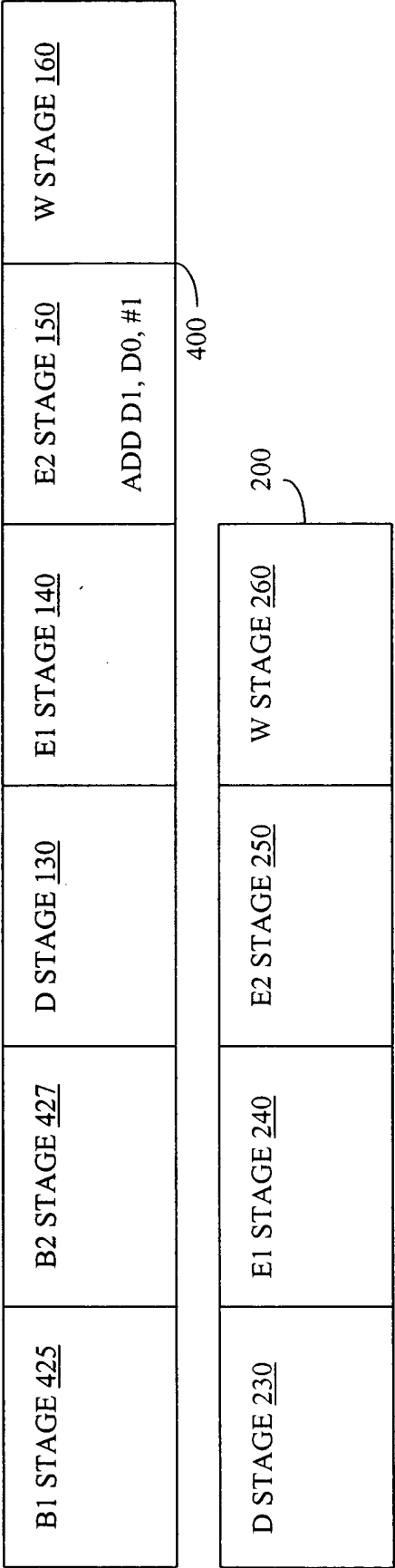


Figure 5(e)

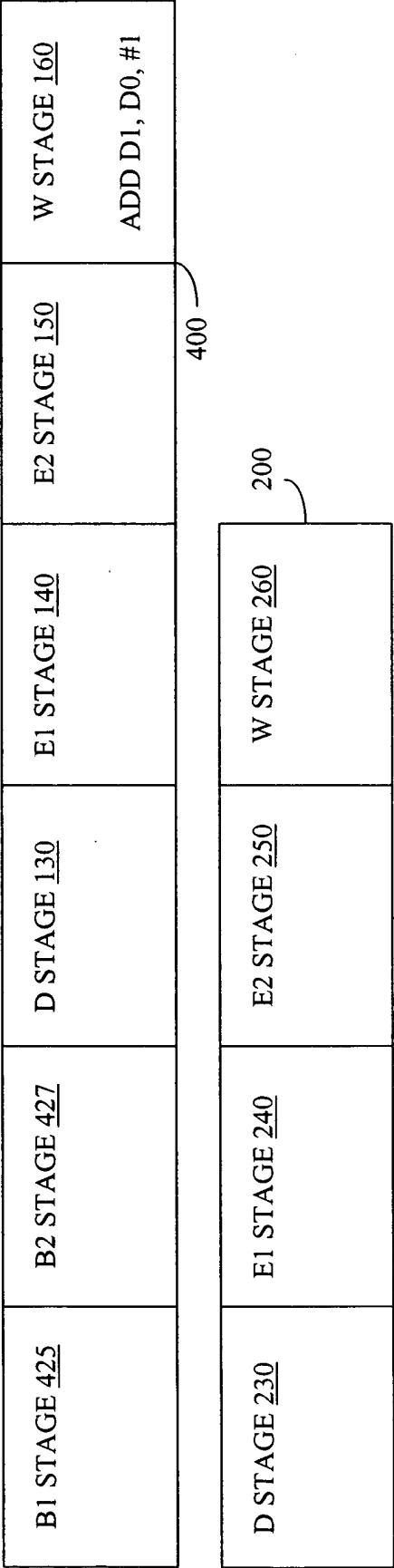


Figure 5(f)

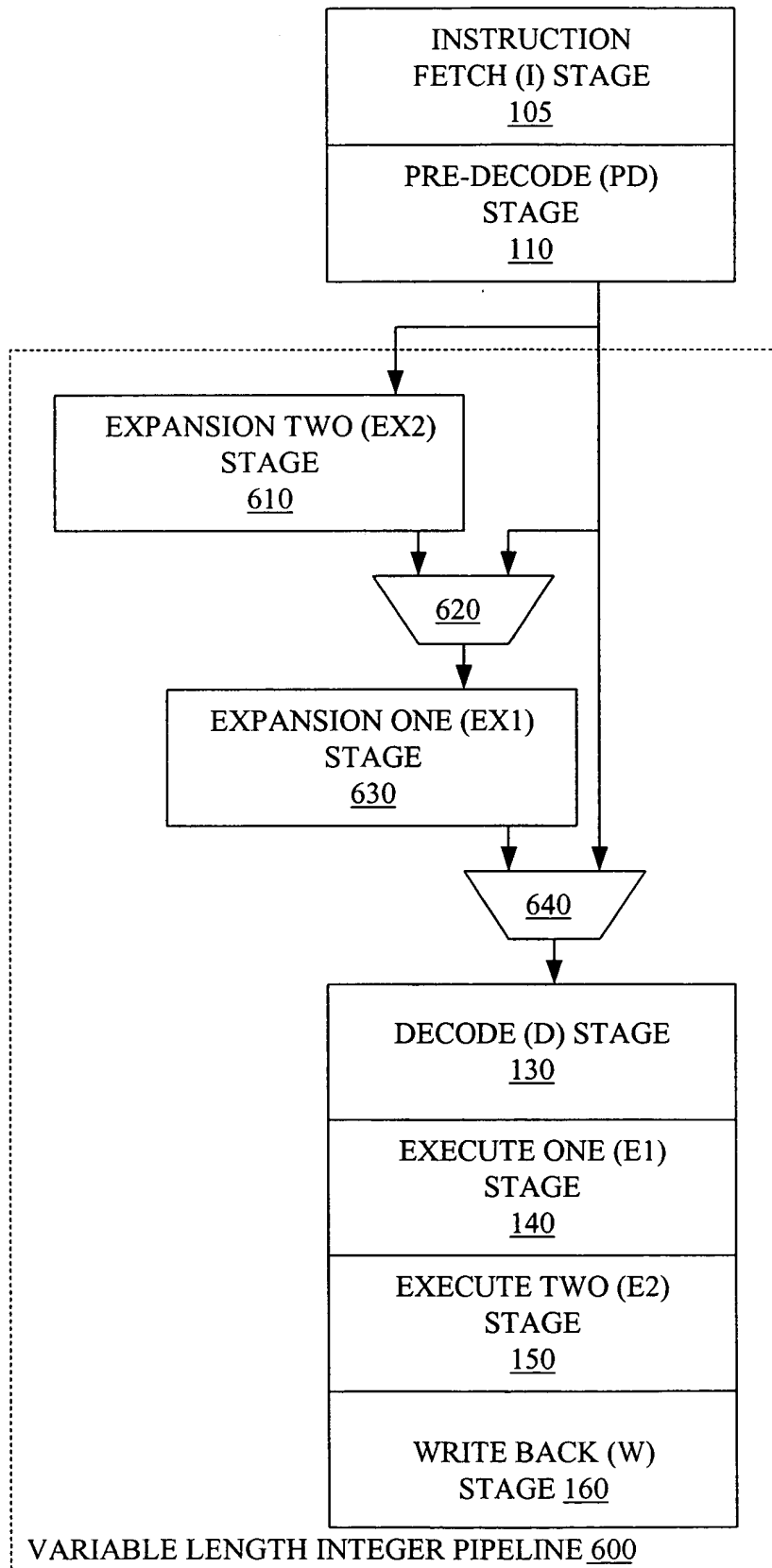


FIGURE 6

D STAGE <u>130</u> SUB D3, D1, #1	E1 STAGE <u>140</u>	E2 STAGE <u>150</u>	W STAGE <u>160</u>
D STAGE <u>230</u> LD D0, [A1]	E1 STAGE <u>240</u>	E2 STAGE <u>250</u>	W STAGE <u>260</u>

D STAGE <u>130</u> ADD D3, D0, #1	E1 STAGE <u>140</u> SUB D3, D1, #1	E2 STAGE <u>150</u>	W STAGE <u>160</u>
D STAGE <u>230</u> LD D0, [A2]	E1 STAGE <u>240</u> LD D0, [A1]	E2 STAGE <u>250</u>	W STAGE <u>260</u>

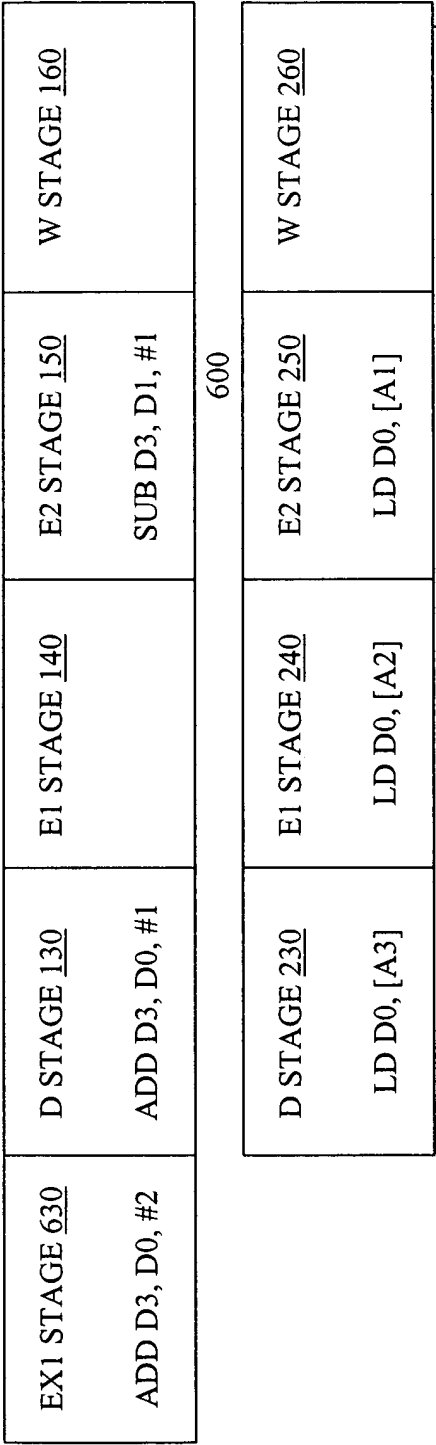


Figure 7(c)

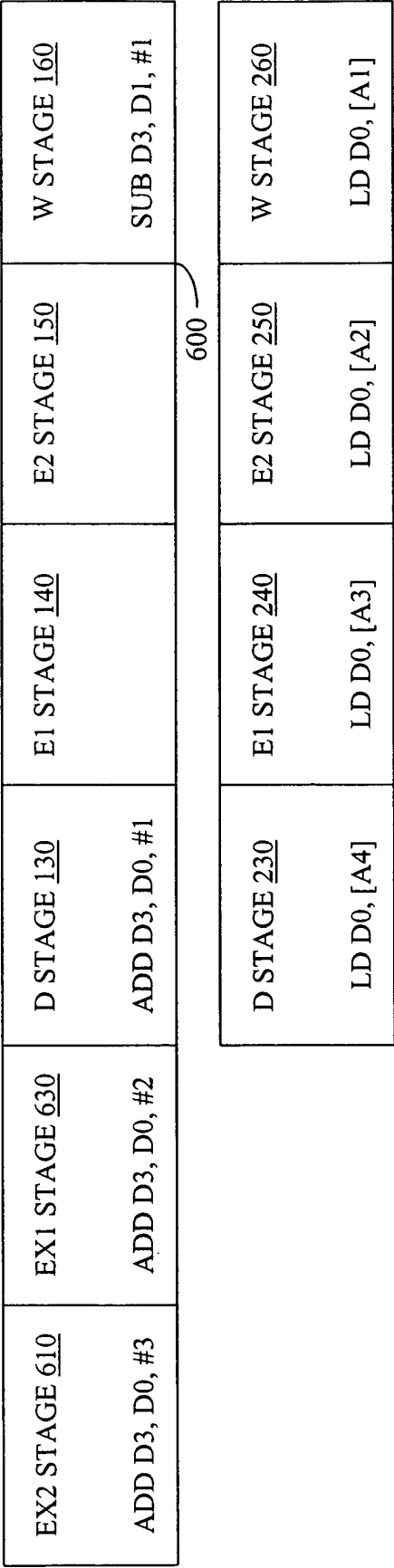


Figure 7(d)

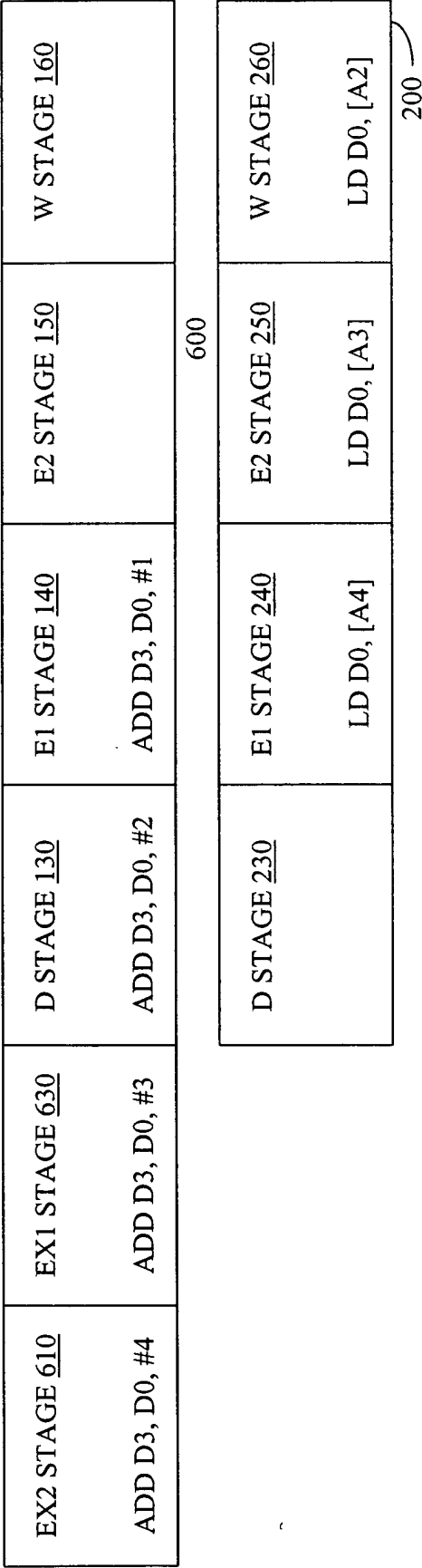


Figure 7(e)

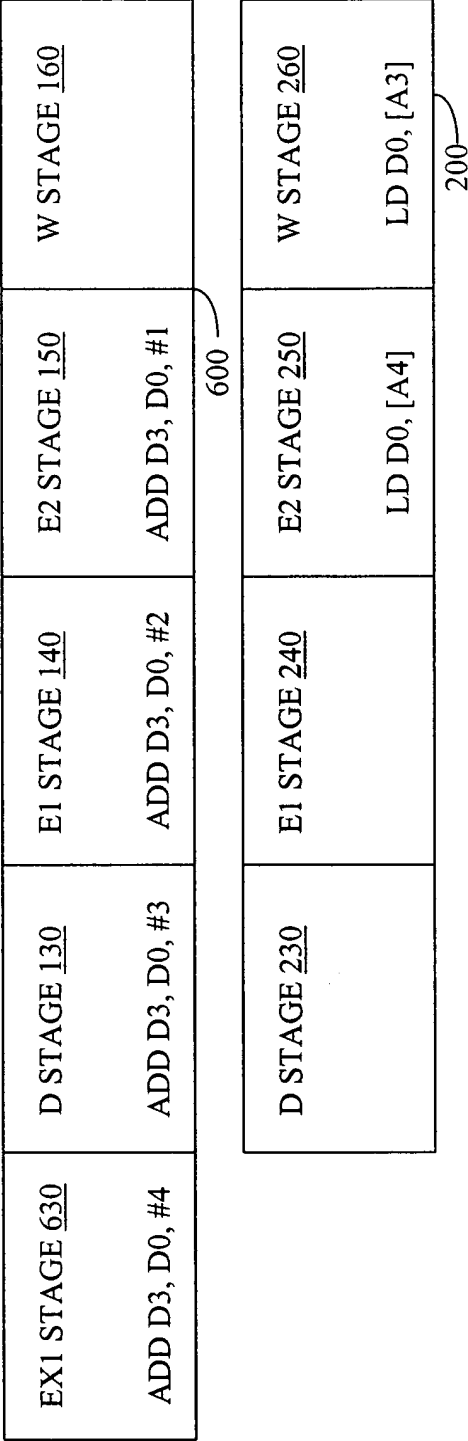


Figure 7(f)

D STAGE <u>130</u> ADD D3, D0, #4	E1 STAGE <u>140</u> ADD D3, D0, #3	E2 STAGE <u>150</u> ADD D3, D0, #2	W STAGE <u>160</u> ADD D3, D0, #1
600			
D STAGE <u>230</u>	E1 STAGE <u>240</u>	E2 STAGE <u>250</u>	W STAGE <u>260</u> LD D0, [A4]
200			

D STAGE <u>130</u>	E1 STAGE <u>140</u> ADD D3, D0, #4	E2 STAGE <u>150</u> ADD D3, D0, #3	W STAGE <u>160</u> ADD D3, D0, #2
600			
D STAGE <u>230</u>	E1 STAGE <u>240</u>	E2 STAGE <u>250</u>	W STAGE <u>260</u>
200			

D STAGE <u>130</u>	E1 STAGE <u>140</u>	E2 STAGE <u>150</u>	W STAGE <u>160</u> ADD D3, D0, #3
600			
D STAGE <u>230</u>	E1 STAGE <u>240</u>	E2 STAGE <u>250</u>	W STAGE <u>260</u>

D STAGE <u>130</u>	E1 STAGE <u>140</u>	E2 STAGE <u>150</u>	W STAGE <u>160</u> ADD D3, D0, #4
600			
D STAGE <u>230</u>	E1 STAGE <u>240</u>	E2 STAGE <u>250</u>	W STAGE <u>260</u>
200			